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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/351,544	07/12/1999	TIMOTHY K. CARNS	ZIL-204	9910

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/351,544	CARNS ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/23/05.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 3-11,36-39,72-74,102-106 and 109-114 is/are pending in the application.

4a) Of the above claim(s) 109-114 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 3-11,36-39,72-74 and 102-106 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3, 8-11, 36, 39, 74 and 102-105 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nariani (U.S. Patent No. 5,470,775) in view of Jacobs et al. (U.S. Patent No. 4,240,196) and further in view of Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109).

With regard to claim 3, Nariani teach a method of forming a capacitor in an integrated circuit comprising:

- forming a lower electrode layer 26/27 on a semiconductor body 20 (figure 2);
- forming a dielectric layer 28 over a portion of the lower electrode layer (figure 2);
- forming an upper electrode layer 29 over a portion of the dielectric layer (figure 2);
- removing a portion of the upper electrode layer 29 to expose a portion of the dielectric layer 28, thereby forming an upper electrode 129with a lateral boundary, wherein a portion of the dielectric layer 28 is disposed in an inter-electrode region, the inter-electrode region disposed within the lateral boundary of the upper electrode 129 and between the lower electrode layer 26/27 and the

upper electrode 129 (intermediate step between figure 2 and 3, the upper electrode layer must necessarily be removed first, thereby necessarily exposing the dielectric layer 28 so that the exposed portions of the dielectric layer can be removed); and

- subsequently removing a portion of the exposed portion of the dielectric layer 28 to expose a portion of the lower electrode layer 26/27 (figure 3).

Nariani does not explicitly teach a portion of the dielectric layer is removed from the inter-electrode region, subsequently forming a conformal insulating layer or forming an anti-reflective layer (ARL) over a portion of the conformal insulating layer. Nariani teach on column 3 lines 44-53 that a conventional mask and etch process is used to form the top electrode 129 and dielectric region 128. Thus, Nariani teach removing the portion of the upper electrode and exposed dielectric layer using conventional processes, but Nariani fails to explicitly teach what the conventional mask and etch process comprises.

Jacobs teaches a method for forming two-level polysilicon devices such as capacitors. Jacobs teaches in figure 2 that undercutting of an oxide layer 12 underneath a polysilicon layer 14 occurs during standard (conventional) etching and processing of the layers. Thus, Jacobs teach that an undercut necessarily occurs in the oxide beneath the polysilicon. This teaching applied to the process of Nariani teaches that Nariani would necessarily remove a portion of the dielectric layer from the inter-electrode region when using conventional processing. Thus, though Nariani does not explicitly disclose removing a portion of the dielectric layer from the inter-electrode

region, Nariani does teach this limitation since this would necessarily occur in their process.

Jacobs further teach in figure 3 forming a conformal insulating layer 18/20 is formed over the structure wherein a portion of the conformal insulating layer 18/20 is formed in the undercut region. In applying the conformal insulating layer (reoxidized layer) of Jacobs into the process of Nariani, the conformal insulating layer would obviously be over a portion of the exposed portion of the lower electrode layer proximate to the portion of the dielectric layer disposed in the inter-electrode region, whereby a portion of the conformal insulating layer is formed in the inter-electrode region. At the time of the invention it would have been obvious to one of ordinary skill in the art to use the conformal insulating layer in the undercut as taught by Jacobs in the method of Nariani in order to reduce breakdown voltage problems as taught by Jacobs (abstract, for example).

Nariani with Jacobs are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the antireflective layer of Bencher in the method of Nariani and Jacobs in order to improve the photolithographic process by reducing net linewidth variations as is well known in the art.

With regard to claim 8, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 9, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 10, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 11, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein plasma enhanced chemical vapor deposition anti-reflective layer (PEARL) has a thickness of 300 angstroms.

With regard to claim 36, Nariani teach:

- forming a conductive layer 26/27 on a semiconductor body (figure 2);
- forming a capacitor structure, comprising:
    - a top electrode 129 over a portion of the conductive layer, wherein the top electrode has a lateral boundary; and
    - a dielectric 128 layer between the top electrode and the conductive layer (figure 3)
- forming a patterned mask over the structure (column 3 lines 57-63 teach using a conventional mask and etch, as is well known in the art a convention mask and etch process will include a patterned mask); and
- etching the conductive layer 26/27 using the patterned mask (figure 4).

As explained above with regard to claim 3, Nariani do not explicitly disclose forming an undercut in the dielectric layer or forming a conformal insulating layer. Nonetheless, as taught by Jacobs, the dielectric layer in an inter-electrode region would be undercut in the conventional process used by Nariani, thus Nariani implicitly teaches this limitation. Also, as explained above, it would have been obvious to use the conformal insulating layer of Nariani in the method of Jacobs.

Nariani with Jacobs are silent to teaching forming an anti-reflective layer (ARL) for use in a lithographic process over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the antireflective layer of Bencher in the method of Nariani and Jacobs in order to improve the photolithographic process by reducing net linewidth variations as is well known in the art.

With regard to claim 39, the conductive layer of Nariani is additionally used to form a gate of one or more transistors formed on the integrated circuit.

With regard to claim 74, Bencher teaches in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

With regard to claim 102, Nariani teaches etching using conventional processes but does not explicitly teach what process is used. Jacobs provides evidence that it is conventional to remove the dielectric layer using isotropic wet etching (column 3 line 39, for example).

With regard to claim 103, Nariani teach a method comprising:

- forming a lower electrode layer 26/27 upon an underlying layer 25 of a semiconductor device 20 (figure 2);
- forming a capacitor dielectric layer 28 (figure 2);
- forming an upper electrode layer 29 wherein the capacitor dielectric layer 28 is disposed in an inter-electrode region between the lower electrode layer 26/27 and the upper electrode layer 29 (figure 2);
- removing a portion of the upper electrode layer 29 such that an upper electrode 129 is formed having an edge (figure 3); and
- removing a portion of the dielectric layer 28 such that an exposed portion of the lower electrode layer 26/27 is formed (figure 3).

Nariani does not explicitly teach an undercutting is formed in the inter-electrode region underneath the edge of the upper electrode wherein the dielectric layer is absent from the undercutting, providing a conformal insulating layer that fills the undercutting or forming an anti-reflective layer (ARL) over a portion of the conformal insulating layer. Nariani teach on column 3 lines 44-53 that a conventional mask and etch process is used to form the top electrode 129 and dielectric region 128. Thus, Nariani teach removing the portion of the upper electrode and exposed dielectric layer using conventional processes, but Nariani fails to explicitly teach what the conventional mask and etch process comprises.

Jacobs teaches a method for forming two-level polysilicon devices such as capacitors. Jacobs teaches in figure 2 that undercutting of an oxide layer 12 underneath a polysilicon layer 14 occurs during standard (conventional) etching and processing of the layers. Thus, Jacobs teach that an undercut necessarily occurs in the oxide beneath the polysilicon. This teaching applied to the process of Nariani teaches that Nariani would necessarily remove a portion of the dielectric layer from the inter-electrode region when using conventional processing. Thus, though Nariani does not explicitly disclose removing a portion of the dielectric layer from the inter-electrode region, Nariani does teach this limitation since this would necessarily occur in their process.

Jacobs further teach in figure 3 forming a conformal insulating layer 18/20 is formed over the structure wherein a portion of the conformal insulating layer 18/20 is formed in the undercut region. In applying the conformal insulating layer (reoxidized layer) of Jacobs into the process of Nariani, the conformal insulating layer would obviously be over a portion of the exposed portion of the lower electrode layer proximate to the portion of the dielectric layer disposed in the inter-electrode region, whereby a portion of the conformal insulating layer is formed in the inter-electrode region. At the time of the invention it would have been obvious to one of ordinary skill in the art to use the conformal insulating layer in the undercut as taught by Jacobs in the method of Nariani in order to reduce breakdown voltage problems as taught by Jacobs (abstract, for example).

Nariani with Jacobs are silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the antireflective layer of Bencher in the method of Nariani and Jacobs in order to improve the photolithographic process by reducing net linewidth variations as is well known in the art.

With regard to claim 104, the capacitor dielectric of Nariani is not disclosed as being 300 to 800 angstroms in thickness. Nonetheless, this claimed range is considered well known and obvious to one of ordinary skill in the art. The claimed thickness is achieved by routine optimization to provide a desired programming voltage and charge storage time of the capacitor and does not provide any unexpected result over the prior art. The claimed range is prima facie obvious without showing that the claimed ranges achieves unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In

re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

With regard to claim 105, the underlying layer 25 electrically isolated the lower electrode layer.

3. Claims 4 – 7, 37, 38, and 106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nariani, Jacobs and Bencher as applied to claims 3, 8-11, 36, 39, 74 and 102-105, respectively, above, and further in view of Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Jacobs teach on column 3 lines 46-50 wherein the conformal insulating layer is oxide. Nariani, Jacobs and Bencher are silent to the conformal insulating layer having a thickness in ranging from 20 angstroms to 70 angstroms. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Nariani with Jacobs and Bencher in order to form a material of high dielectric constant that is compatible with ULSI polysilicon processing as stated by Wang in column 1, lines 16 – 17, column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, similar to the rejection of claim 4, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Nariani, Jacobs, Bencher and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal process that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C to form the conformal insulating layer of Nariani, Jacobs, Bencher and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, similar to the rejection of claim 4, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

With regard to claims 37, Nariani with Jacobs and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Nariani, Jacobs and Bencher in

order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 38, similar to the rejection of claim 37, above, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 106, similar to claims 4 and 6 above, Nariani with Jacobs and Bencher in view of Wang teach wherein the providing the conformal insulating layer in step (f) is performed using a rapid thermal oxidation (RTO) process to grow a layer of silicon oxide to a thickness ranging from 20 angstroms to 100 angstroms.

4. Claims 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nariani with Jacobs and Bencher as applied to claim 3 above, and further in view of Jain et al. (USPAT 5741626, Jain).

With regard to claim 72, Nariani with Jacobs and Bencher, as combined in claim 3, teach forming a photoresist mask over a portion of the anti-reflective layer (ARL). Nariani with Jacobs and Bencher, as combined in claim 3, teach irradiating the photoresist with radiation that penetrates the photoresist mask. It is not clear if Nariani with Jacobs and Bencher teach wherein the antireflective layer reduces a reflection of the radiation by 70% or more. Jain teaches in figure7, as compared to figure 6, wherein an antireflective layer reduces a reflection of radiation by 70% or more (i.e. 100% minus 15% divided by 93% times 100% is equal to an 84 % reduction in reflectivity). It would have been obvious to use the antireflective layer of Jain in the method of Nariani with

Jacobs and Bencher, as combined in claim 3, in order to decrease distortion while patterning the photoresist as stated by Jain in the abstract.

With regard to claim 73, the Jain teaches in figure 7, as compared to figure 6, wherein the anti-reflective layer reduces the reflection of the radiation by 84%.

Response to Arguments

5. Applicant's arguments with respect to claims 3-11, 36-39, 72-74 and 102-106 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

TOM THOMAS
SUPERVISORY PATENT EXAMINER